Challenges for Interconnect Simulation in High Speed Digital Board and System Design

A Proposal for Solving the High Speed Design Puzzle

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Outline

Introduction:
- Special demands of high speed digital design
- General trends of board design
- High speed design paradigm of today and tomorrow

Interconnect Simulation in Design Process of Tomorrow:
- Stages during the design process
- Demands

Demands for the CAE-Environment
- Providing a complete electrical database
- Additional expert system

Conclusion
- Solving the high speed puzzle
Special Demands of High Speed Digital Board Design: Timing

Higher Clock Frequencies

<table>
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<th>Year</th>
<th>f</th>
<th>t_clock</th>
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<tbody>
<tr>
<td>1985</td>
<td>16 MHz</td>
<td>60 ns</td>
</tr>
<tr>
<td>1995</td>
<td>120 MHz</td>
<td>8 ns</td>
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Shorter Internal Delays

<table>
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<tr>
<th>Year</th>
<th>t_prop</th>
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</thead>
<tbody>
<tr>
<td>1985</td>
<td>45 ns</td>
</tr>
<tr>
<td>1995</td>
<td>5 ns</td>
</tr>
</tbody>
</table>

Shorter Delay Margins

Interconnect Simulation in High Speed Digital Design

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Special Demands of High Speed Digital Board Design: Signal Integrity (SI)

- Shorter Transition Times
- More Overshoot
- More Reflexions
- More Xtalk

Interconnect Simulation in High Speed Digital Design

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General Trends of Board Design

Higher Integration, Smaller Structures
- more nets per board
- higher density of signal lines

Reducing Supply Voltage
- more restricted noise margins

Time to Market
- first time right
- verification by simulation of total board

Use Automatization wherever possible
High Speed Digital Board Design Paradigm of Today: Overview

Interconnect Simulation in High Speed Digital Design
High Speed Digital Board Design Paradigm of Today: Drawbacks I

Identifying Critical Nets based on Schematic

Usually manual work
• Possible classifying error
• Some nets may get critical during placement

Setting Up Geometric Rules for Critical Nets

• More restrictive than necessary
• Commonly fixed in handwritten notes
• Not adaptable
• Topology rules not easily implemented
• Crosstalk clearance rules can't account for differences in near end and far end crosstalk
High Speed Digital Board Design Paradigm of Today: Drawbacks II

Observing Geometrical Rules during Layout
- Realization of handwritten notes is time-consuming
- No solution, if placement couldn't observe rules
- Simple delay calculation based on line length, but: real net delays can exceed these values by far due to reflexions.

Double Checking all Nets after Layout
- In case of mistake another layout iteration is necessary:
  - No guarantee of success
  - Possible damage of other critical nets

Wasting Time and Money
- A new high speed design paradigm is needed

Interconnect Simulation in High Speed Digital Design
High Speed Digital Board Design Paradigm of Tomorrow

- Schematic
  - Automatic optimization of net topologies and terminations
- Layout
  - Automatic placement for observing signal integrity and timing
- Placement
- Routing
  - Realtime interconnect simulation during routing guarantees:
    - Signal integrity
    - Timing with propagation effects
    - Xtalk (correct near/far end)
- Production

ADDITIONAL HIGH SPEED ACTIONS
- Automatic identification of critical nets
- Automatic suggestions for improvement

⇒ 'First time right' layout
Stages of Interconnect Simulation during the Design Process of Tomorrow

- Schematic
  - Feasibility: technology selection
  - Identifying critical nets
  - Generation of rules
- Layout
  - Verifying placement
  - Fixing signal integrity and delay
- Placement
  - Checking signal integrity, timing and crosstalk
- Routing
  - Postlayout: double checking
- Production
  - INTERCONNECT SIMULATION
Weak and strong types of I/Os generally differ a lot. Don't be "overexact".

Demands for the Interconnect Simulation Environment

Before Routing:
- Based on Manhattan length
- Easy changes of driver technology, net topology and termination

During Routing:
- Realtime
- Crosstalk: all driver/receiver combinations

Multiboard: appropriate 'phantom' driver/receivers

Demands for the Interconnect Simulator
Interconnect Simulation Environment of Today

Simple and Fast Transmission Line Simulation

- simple behavioural models of I/Os
- simple LC-models of vias, packages, connectors
- transmission line parameters only with DC-losses
  \[ f_{\text{clock}} < 200 \text{ MHz} \]

or

High Precision Simulation

- physical models
- complex models of vias, packages, connectors
- transmission line parameters with DC&AC-losses
  time consuming
Demands for the Interconnect Simulation Environment

- Refined behavioural models of I/Os (target: 800MHz)
- DC & AC line losses
- Behavioural models of special components, e.g., cables
- Physical models if necessary
- Integrate results of ΔI-noise calculation
- Fast board simulation
- Detailed modelling of vias, packages, connectors
- Arbitrary line shapes
- Non perfect power/ground planes
Demands for the CAE-Environment

Providing a Complete Electrical Database:
• Parameters for splitted powerplanes
• Models for cables
• All electrical parameters of the board (frequency dependent)
• Handling arbitrary line shapes (2.5-D-field-analysis)

Additional Expert System:
• Automatic classification of critical nets
• Predefined set of rules for fixing signal integrity
• Learning by testing various strategies for fixing SI
Conclusion

Solving the Designers High Speed Puzzle

Fast Interconnect Simulator

Reusable Set of Rules

Tactical Router

Layout System

Expert System

Solving the Designers High Speed Puzzle